Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of the Claims

1. (Currently Amended) An apparatus comprising:

an analog to digital converter for generating a digital signal in response to a first clock signal;

a fixed rate clock generator for generating said ~~a source of a~~ first clock ~~input~~ signal;

a phased lock loop for generating a ~~source of a~~ second clock ~~input~~ signal in response to said first clock signal;

a delay means comprising a plurality of outputs for delaying the first clock ~~input~~ signal responsive to the second clock ~~input~~ signal; ~~and~~

a means to compare said plurality of outputs of the delay means to produce a first output signal, wherein the first output signal produced is a synchronization of the first clock signal and the second clock signal; and

a processing means to process said digital signal in response to said first output signal.

2. (Cancelled)

3. (Cancelled)

4. (previously presented) The apparatus of claim 1 wherein the delay means comprises a plurality of flip-flops.

5. (previously presented) The apparatus of claim 1 wherein a plurality of comparisons are made between a plurality of the outputs of the delay means to produce multiple output signals.

6. (previously presented) The apparatus of claim 2 wherein the output signal is a clock signal with a 50% duty cycle.

7. (previously presented) An apparatus comprising:

a first input to receive a first clock signal;

a second input to receive a second clock signal;

an output;

a first flip-flop wherein the first clock signal is connected to a data input of the first flip-flop and the second clock signal is connected to a clock input of the first flip-flop;

a second flip-flop wherein an output of the first flip-flop is connected a data input of the second flip-flop and the second clock signal is connected to a clock input of the second flip-flop;

a third flip-flop wherein an output of the second flip-flop is connected a data input of the third flip-flop and the second clock signal is connected to a clock input of the third flip-flop;

a fourth flip-flop wherein an output of the third flip-flop is connected a data input of the fourth flip-flop and the second clock signal is connected to a clock input of the fourth flip-flop;

a fifth flip-flop wherein an output of the fourth flip-flop is connected a data input of the fifth flip-flop and the second clock signal is connected to a clock input of the fifth flip-flop;

a first AND gate where the output of the first flip-flop is connected to a first input of the first AND gate and the output of the second flip-flop is connected to a second input of the first AND gate;

a second AND gate where the output of the fourth flip-flop is connected to a first input of the second AND gate and the output of the fifth flip-flop is connected to a second input of the second AND gate;

a first or gate where the output of the first AND gate is connected to the first input of the first OR gate and the output of the second AND gate is connected to the second input of the first OR gate; and

a sixth flip-flop where the output of the first OR gate is connected to the D input of the sixth flip-flop and the second input is connected to the clock input of the sixth flip-flop and the output of the sixth flip-flop is connected to the output of the apparatus for producing a first output signal.

8. (previously presented) The apparatus of claim 7 wherein the first output signal produced is a synchronization of the first input signal and the second input signal.

9. (previously presented) The apparatus of claim 8 wherein the first clock signal at the first input is a fixed rate clock signal and the second clock signal at the second input is a clock signal derived from a phase locked loop.

10. (previously presented) The apparatus of claim 9 wherein the first output signal is a clock signal with a 50% duty cycle.

11. (currently amended) A method for processing an analog ~~for synchronizing a first clock signal and a second clock~~ signal comprising the steps of:

generating a first digital signal from a first analog signal in response to a first clock signal;

generating a second clock signal in response to said first clock signal;

passing said first clock signal through a delay means having a plurality of outputs wherein said delay means is responsive to said second clock signal; ~~and~~

comparing two or more of the plurality of outputs of the delay means to produce a first output signal wherein the first output signal produced is a synchronization of the first clock signal and the second clock signal; and

processing said first digital signal in response to said first output signal.

12. (previously presented) The method of claim 11 wherein the comparing of two or more of the plurality of outputs of the delay means is performed using logic devices.

13. (previously presented) The method of claim 11 wherein the comparing of two or more of the plurality of outputs of the delay means is performed using software.

14. (previously presented) The method of claim 11 wherein the signal at the first clock signal is a fixed rate clock signal and the second clock signal is a clock signal derived from a phase locked loop.

15. (previously presented) The method of claim 11 wherein the delay means comprises a plurality of flip-flops.

16. (previously presented) The method of claim 11 wherein a plurality of comparisons are made between a plurality of the outputs of the delay means to produce multiple output signals.